IN THE CLAIMS:

Kindly amend the claims, as follows:

1. (Currently Amended) A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that transmits a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial control data ~~gate~~ signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

2. (Currently Amended) ~~The latency-independent interface of claim 1,~~ A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that transmits a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

3. (Currently Amended) The latency-independent interface of claim [[1]] 2, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

4. (Currently Amended) The latency-independent interface of claim [[1]] 2, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

5. (Currently Amended) ~~The latency-independent interface of claim 1,~~ A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that transmits a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

6. (Currently Amended) ~~The latency-independent interface of claim 1,~~ A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that transmits a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises [[a]] information if a succeeding serial control data is a continuation of a current serial control data.

7. (Currently Amended) The latency-independent interface of claim [[1]] 2, wherein the serial control data signal comprises

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

8. (Currently Amended) ~~The latency-independent interface of claim 1,~~ A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that transmits a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising a ready transceiver that transmits or receives a bi-directional ready signal.

9. (Currently Amended) The latency-independent interface of claim [[1]] 2, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

10. (Currently Amended) The latency-independent interface of claim [[1]] 2, further comprising a sync mark transceiver that transmits or receives sync mark information.

11. (Original) The latency-independent interface of claim 10, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

12. – 14. (Canceled)

15. (Original) A latency-independent interface between first and second hardware components, comprising:

serial control transmitting means for transmitting a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

16. (Currently Amended) ~~The latency-independent interface of claim 15,~~ A latency-independent interface between first and second hardware components, comprising:

serial control transmitting means for transmitting a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

17. (Currently Amended) The latency-independent interface of claim ~~15~~ 16, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

18. (Currently Amended) The latency-independent interface of claim ~~15~~ 16, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

19. (Currently Amended) ~~The latency-independent interface of claim 15,~~ A latency-independent interface between first and second hardware components, comprising:

serial control transmitting means for transmitting a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

20. (Currently Amended) ~~The latency-independent interface of claim 15,~~ A latency-independent interface between first and second hardware components, comprising:

serial control transmitting means for transmitting a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises [[a]] information if a succeeding serial control data is a continuation of a current serial control data.

21. (Currently Amended) The latency-independent interface of claim ~~15~~ 16, wherein the serial control data signal comprises

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

22. (Currently Amended) ~~The latency-independent interface of claim 15,~~ A latency-independent interface between first and second hardware components, comprising:

serial control transmitting means for transmitting a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising a ready transceiver means for transmitting or receiving a bi-directional ready signal.

23. (Currently Amended) The latency-independent interface of claim ~~15~~ 16, wherein the first hardware component comprises disk controller means and the second hardware component comprises read channel means.

24. (Currently Amended) The latency-independent interface of claim ~~15~~ 16, further comprising a sync mark transceiver means for transmitting or receiving sync mark information.

25. (Original) The latency-independent interface of claim 24, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

26. – 30. (Canceled)

31. (Original) A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

32. (Currently Amended) ~~The method of claim 31,~~ A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

33. (Currently Amended) The method of claim ~~31~~ 32, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

34. (Currently Amended) The method of claim ~~31~~ 32, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

35. (Currently Amended) ~~The method of claim 31,~~ A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

36. (Currently Amended) ~~The method of claim 31,~~ A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

37. (Currently Amended) The method of claim ~~31~~ 32, wherein the serial control data signal comprises:

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

38. (Currently Amended) ~~The method of claim 31,~~ A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising the step of transmitting or receiving a bi-directional ready signal.

39. (Currently Amended) The method of claim ~~31~~ 32, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

40. (Currently Amended) The method of claim ~~31~~ 32, further comprising the step of transmitting or receiving sync mark information.

41. (Original) The method of claim 40, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

42. – 45. (Canceled)

46. (Original) A latency-independent interface between first and second hardware

components, comprising:

a serial control data circuit that receives a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial data gate signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

47. (Currently Amended) ~~The latency-independent interface of claim 46,~~ A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that receives a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial data gate signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

48. (Currently Amended) The latency-independent interface of claim ~~46~~ 47, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

49. (Currently Amended) The latency-independent interface of claim ~~46~~ 47, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

50. (Currently Amended) ~~The latency-independent interface of claim 46,~~ A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that receives a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial data gate

signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

51. (Currently Amended) ~~The latency-independent interface of claim 46,~~ A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that receives a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial data gate signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

52. (Currently Amended) The latency-independent interface of claim ~~46~~ 47, wherein the serial control data signal comprises:

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

53. (Currently Amended) ~~The latency-independent interface of claim 46,~~ A latency-independent interface between first and second hardware components, comprising:

a serial control data circuit that receives a serial control data signal; and

a data circuit that transmits or receives data under the control of the serial data gate signal,

wherein the serial control data signal comprises information as to whether the

data is one of split and non-split, and

further comprising a ready transceiver that transmits or receives a bi-directional ready signal.

54. (Currently Amended) The latency-independent interface of claim ~~46~~ 47, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

55. (Currently Amended) The latency-independent interface of claim ~~46~~ 47, further comprising a sync mark transceiver that transmits or receives sync mark information.

56. (Original) The latency-independent interface of claim 55, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

57. – 59. (Canceled)

60. (Original) A latency-independent interface between first and second hardware components, comprising:

serial control receiving means for receiving a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

61. (Currently Amended) ~~The latency-independent interface of claim 60,~~ A latency-independent interface between first and second hardware components, comprising:

serial control receiving means for receiving a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

62. (Currently Amended) The latency-independent interface of claim ~~60~~ 61, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

63. (Currently Amended) The latency-independent interface of claim ~~60~~ 61, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

64. (Currently Amended) ~~The latency-independent interface of claim 60,~~ A latency-independent interface between first and second hardware components, comprising:

serial control receiving means for receiving a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

65. (Currently Amended) ~~The latency-independent interface of claim 60,~~ A latency-independent interface between first and second hardware components, comprising:

serial control receiving means for receiving a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

66. (Currently Amended) The latency-independent interface of claim ~~60~~ 61, wherein the serial control data signal comprises

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

67. (Currently Amended) ~~The latency-independent interface of claim 60,~~ A latency-independent interface between first and second hardware components, comprising:

serial control receiving means for receiving a serial control data signal; and

data transceiver means for transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising a ready transceiver means for transmitting or receiving a bi-directional ready signal.

68. (Currently Amended) The latency-independent interface of claim ~~60~~ 61, wherein the first hardware component comprises disk controller means and the second hardware component comprises read channel means.

69. (Currently Amended) The latency-independent interface of claim ~~60~~ 61, further comprising a sync mark transceiver means for transmitting or receiving sync mark information.

70. (Original) The latency-independent interface of claim 69, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

71. – 75. (Canceled)

76. (Original) A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

77. (Currently Amended) ~~The method of claim 76,~~ A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

78. (Currently Amended) The method of claim ~~76~~ 77, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

79. (Currently Amended) The method of claim ~~76~~ 77, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

80. (Currently Amended) ~~The method of claim 76,~~ A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

81. (Currently Amended) ~~The method of claim 76,~~ A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

82. (Currently Amended) The method of claim ~~76~~ 77, wherein the serial control data signal comprises

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

83. (Currently Amended) ~~The method of claim 76,~~ A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising the step of transmitting or receiving a bi-directional ready signal.

84. (Currently Amended) The method of claim ~~76~~ 77, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

85. (Currently Amended) The method of claim ~~76~~ 77, further comprising the step of transmitting or receiving sync mark information.

86. (Original) The method of claim 85, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

87. – 90. (Canceled)

91. (Original) A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

92. (Currently Amended) ~~The computer program of claim 91,~~ A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

93. (Currently Amended) The computer program of claim ~~91~~ 92, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

94. (Currently Amended) The computer program of claim ~~91~~ 92, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

95. (Currently Amended) ~~The computer program of claim 91,~~ A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current

sector.

96. (Currently Amended) ~~The computer program of claim 91,~~ A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

97. (Currently Amended) The computer program of claim ~~91~~ 92, wherein the serial control data signal comprises:

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

98. (Currently Amended) ~~The computer program of claim 91,~~ A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising the step of transmitting or receiving a bi-directional ready signal.

99. (Currently Amended) The computer program of claim ~~91~~ 92, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

100. (Currently Amended) The computer program of claim ~~91~~ 92, further comprising the step of transmitting or receiving sync mark information.

101. (Original) The computer program of claim 100, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

102. – 105. (Canceled)

106. (Original) A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

107. (Currently Amended) ~~The computer program of claim 106,~~ A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

108. (Currently Amended) The computer program of claim ~~106~~ 107, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

109. (Currently Amended) The computer program of claim ~~106~~ 107, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

110. (Currently Amended) ~~The computer program of claim 106,~~ A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

111. (Currently Amended) ~~The computer program of claim 106,~~ A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises [[a]] information if a succeeding serial control data is a continuation of a current serial control data.

112. (Currently Amended) The computer program of claim ~~106~~ 107, wherein the serial control data signal comprises:

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

113. (Currently Amended) ~~The computer program of claim 106,~~ A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal; and

transmitting or receiving data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising the step of transmitting or receiving a bi-directional ready signal.

114. (Currently Amended) The computer program of claim ~~106~~ 107, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

115. (Currently Amended) The computer program of claim ~~106~~ 107, further comprising the step of transmitting or receiving sync mark information.

116. (Original) The computer program of claim 115, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark

insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

117. – 120. (Canceled)

121. (Original) A data transmission system comprising:

a first component comprising:

a serial control transmitter circuit that transmits a serial control data signal; and

a first data transceiver circuit that transmits or receives data under the control of the serial control data signal,

a second component comprising:

a serial control receiver circuit that receives the serial control data signal; and

a second data transceiver circuit that transmits or receives the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

122. (Currently Amended) ~~The latency independent interface of claim 121,~~ A data transmission system, comprising:

a first component comprising:

a serial control transmitter circuit that transmits a serial control data signal; and

a first data transceiver circuit that transmits or receives data under the control of the serial control data signal; and

a second component comprising:

a serial control receiver circuit that receives the serial control data signal; and

a second data transceiver circuit that transmits or receives the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

123. (Currently Amended) The ~~latency-independent interface~~ data transmission system of claim ~~121~~ 122, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

124. (Currently Amended) The ~~latency-independent interface~~ data transmission system of claim ~~121~~ 122, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

125. (Currently Amended) ~~The latency-independent interface of claim 121,~~ A data transmission system comprising:

a first component comprising:

a serial control transmitter circuit that transmits a serial control data signal; and

a first data transceiver circuit that transmits or receives data under the control of the serial control data signal; and

a second component comprising:

a serial control receiver circuit that receives the serial control data signal; and

a second data transceiver circuit that transmits or receives the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

126. (Currently Amended) ~~The latency-independent interface of claim 121,~~ A data transmission system comprising:

a first component comprising:

a serial control transmitter circuit that transmits a serial control data signal; and

a first data transceiver circuit that transmits or receives data under the control of the serial control data signal; and

a second component comprising:

a serial control receiver circuit that receives the serial control data signal; and

a second data transceiver circuit that transmits or receives the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises [[a]] information if a succeeding serial control data is a continuation of a current serial control data.

127. (Currently Amended) The ~~latency-independent interface~~ data transmission system of claim ~~121~~ 122, wherein the serial control data signal comprises:

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

128. (Currently Amended) ~~The latency-independent interface of claim 121,~~ A data transmission system comprising:

a first component comprising:

a serial control transmitter circuit that transmits a serial control data signal; and

a first data transceiver circuit that transmits or receives data under the control of the serial control data signal; and

a second component comprising:

a serial control receiver circuit that receives the serial control data signal; and

a second data transceiver circuit that transmits or receives the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the first component further comprises a first ready transceiver that transmits or receives a bi-directional ready signal and wherein the second component further comprising a second ready transceiver that transmits or receives the bi-directional ready signal.

129. (Currently Amended) The ~~latency-independent interface~~ data transmission system of claim ~~121~~ 122, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

130. (Currently Amended) The ~~latency-independent interface~~ data transmission system of claim ~~121~~ 122, wherein the first component further comprises a first sync mark transceiver that transmits or receives sync mark information and wherein the second component further comprises a second sync mark transceiver that transmits or receives the sync mark information.

131. (Original) The ~~latency-independent interface~~ data transmission system of claim 130, wherein during a write operation a first assertion of the sync mark information

indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

132. – 134. (Canceled)

135. (Original) A data transmission system comprising:

first component means comprising:

serial control transmitter means for transmitting a serial control data signal; and

first data transceiver means for transmitting or receiving data under the control of the serial control data signal,

second component means comprising:

serial control receiver means for receiving the serial control data signal; and

a second data transceiver means for transmitting or receiving the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

136. (Currently Amended) ~~The latency independent interface of claim 135,~~ A data transmission system comprising:

first component means comprising:

serial control transmitter means for transmitting a serial control data signal; and

first data transceiver means for transmitting or receiving data under the control of the serial control data signal; and

second component means comprising:

serial control receiver means for receiving the serial control data signal; and

a second data transceiver means for transmitting or receiving the data

under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

137. (Currently Amended) The ~~latency-independent interface~~ data transmission system of claim ~~135~~ 136, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

138. (Currently Amended) The ~~latency-independent interface~~ data transmission system of claim ~~135~~ 136, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

139. (Currently Amended) ~~The latency-independent interface of claim 135,~~ A data transmission system comprising:

first component means comprising:

serial control transmitter means for transmitting a serial control data signal; and

first data transceiver means for transmitting or receiving data under the control of the serial control data signal; and

second component means comprising:

serial control receiver means for receiving the serial control data signal; and

a second data transceiver means for transmitting or receiving the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current

sector.

140. (Currently Amended) ~~The latency-independent interface of claim 135,~~ A data transmission system comprising:

first component means comprising:

serial control transmitter means for transmitting a serial control data signal; and

first data transceiver means for transmitting or receiving data under the control of the serial control data signal,

second component means comprising:

serial control receiver means for receiving the serial control data signal; and

a second data transceiver means for transmitting or receiving the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises [[a]] information if a succeeding serial control data is a continuation of a current serial control data.

141. (Currently Amended) The ~~latency-independent interface~~ data transmission system of claim ~~135~~ 136, wherein the serial control data signal comprises

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

142. (Currently Amended) ~~The latency-independent interface of claim 135,~~ A data transmission system comprising:

first component means comprising:

serial control transmitter means for transmitting a serial control data signal; and

first data transceiver means for transmitting or receiving data under the control of the serial control data signal; and

second component means comprising:

serial control receiver means for receiving the serial control data signal; and

a second data transceiver means for transmitting or receiving the data under the control of the serial control data signal,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split,

wherein said first component means further comprises first ready transceiver means for transmitting or receiving a bi-directional ready signal, and

wherein said second component means further comprises second ready transceiver means for transmitting or receiving the bi-directional ready signal.

143. (Currently Amended) The ~~latency-independent interface~~ data transmission system of claim ~~135~~ 136, wherein said first hardware component comprises disk controller means and said second hardware component comprises read channel means.

144. (Currently Amended) The ~~latency-independent interface~~ data transmission system of claim ~~135~~ 136, wherein said first component means further comprises first sync mark transceiver means for transmitting or receiving sync mark information, and wherein said second component means further comprises second sync mark transceiver means for transmitting or receiving the sync mark information.

145. (Original) The ~~latency-independent interface~~ data transmission system of claim 144, wherein during a write operation a first assertion of the sync mark information

indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

146. – 150. (Canceled)

151. (Original) A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

152. (Currently Amended) ~~The method of claim 151,~~ A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

153. (Currently Amended) The method of claim ~~151~~ 152, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

154. (Currently Amended) The method of claim ~~151~~ 152, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

155. (Currently Amended) ~~The method of claim 151,~~ A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

156. (Currently Amended) ~~The method of claim 151,~~ A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

157. (Currently Amended) The method of claim ~~151~~ 152, wherein the serial control data signal comprises

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

158. (Currently Amended) ~~The method of claim 151,~~ A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising the step of transmitting or receiving a bi-directional ready signal by the first component and transmitting or receiving the bi-directional ready signal by the second component.

159. (Currently Amended) The method of claim ~~151~~ 152, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

160. (Currently Amended) The method of claim ~~151~~ 152, further comprising the step of transmitting or receiving sync mark information by the first component, and transmitting or receiving the sync mark information by the second component.

161. (Original) The method of claim 160, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

162. – 211. (Canceled)

212. (Original) A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split.

213. (Currently Amended) ~~The computer program of claim 212,~~ A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by

the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information that the data is one of first split, continue split and last split.

214. (Currently Amended) The computer program of claim ~~212~~ 213, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

215. (Currently Amended) The computer program of claim ~~212~~ 213, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

216. (Currently Amended) ~~The computer program of claim 212,~~ A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises a codeword size of a current sector.

217. (Currently Amended) ~~The computer program of claim 212,~~ A computer program for transmitting and receiving signals between first and second hardware

components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

wherein the serial control data signal comprises information if a succeeding serial control data is a continuation of a current serial control data.

218. (Currently Amended) The computer program of claim ~~212~~ 213, wherein the serial control data signal comprises

during a write operation information as to a start of a sync mark and a start of write padding data, and

during a read operation information that a sync mark was detected.

219. (Currently Amended) ~~The computer program of claim 212,~~ A computer program for transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a serial control data signal from the first component;

receiving the serial control data signal by the second component;

transmitting or receiving data under the control of the serial control data signal by the first component; and

transmitting or receiving the data under the control of the serial control data signal by the second component,

wherein the serial control data signal comprises information as to whether the data is one of split and non-split, and

further comprising the step of transmitting or receiving a bi-directional ready signal by the first component and transmitting or receiving the bi-directional ready signal by the second component.

220. (Currently Amended) The computer program of claim ~~212~~ 213, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

221. (Currently Amended) The computer program of claim ~~212~~ 213, further comprising the step of transmitting or receiving sync mark information by the first component, and transmitting or receiving the sync mark information by the second component.

222. (Original) The computer program of claim 221, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

223. – 248. (Canceled)

249. (New) The latency-independent interface of claim 5, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

250. (New) The latency-independent interface of claim 5, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

251. (New) The latency-independent interface of claim 5, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write

padding data; and

during a read operation, information that a sync mark was detected.

252. (New) The latency-independent interface of claim 5, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

253. (New) The latency-independent interface of claim 5, further comprising:

a sync mark transceiver that transmits or receives sync mark information.

254. (New) The latency-independent interface of claim 253, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

255. (New) The latency-independent interface of claim 6, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

256. (New) The latency-independent interface of claim 6, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

257. (New) The latency-independent interface of claim 6, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

258. (New) The latency-independent interface of claim 6, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

259. (New) The latency-independent interface of claim 6, further comprising:

a sync mark transceiver that transmits or receives sync mark information.

260. (New) The latency-independent interface of claim 259, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

261. (New) The latency-independent interface of claim 8, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

262. (New) The latency-independent interface of claim 8, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

263. (New) The latency-independent interface of claim 8, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

264. (New) The latency-independent interface of claim 8, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

265. (New) The latency-independent interface of claim 8, further comprising:

a sync mark transceiver that transmits or receives sync mark information.

266. (New) The latency-independent interface of claim 265, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark

insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

267. (New) The method of claim 35, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

268. (New) The method of claim 35, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

269. (New) The method of claim 35, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

270. (New) The method of claim 35, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

271. (New) The method of claim 35, further comprising the step of:

transmitting or receiving sync mark information.

272. (New) The method of claim 271, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

273. (New) The method of claim 36, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

274. (New) The method of claim 36, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

275. (New) The method of claim 36, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

276. (New) The method of claim 36, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

277. (New) The method of claim 36, further comprising the step of:

transmitting or receiving sync mark information.

278. (New) The method of claim 277, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

279. (New) The method of claim 38, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

280. (New) The method of claim 38, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

281. (New) The method of claim 38, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

282. (New) The method of claim 38, wherein the first hardware component

comprises a disk controller and the second hardware component comprises a read channel.

283. (New) The method of claim 38, further comprising the step of:
transmitting or receiving sync mark information.

284. (New) The method of claim 283, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

285. (New) The latency-independent interface of claim 50, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

286. (New) The latency-independent interface of claim 50, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

287. (New) The latency-independent interface of claim 50, wherein the serial control data signal comprises:
during a write operation, information as to a start of a sync mark and a start of write padding data; and
during a read operation, information that a sync mark was detected.

288. (New) The latency-independent interface of claim 50, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

289. (New) The latency-independent interface of claim 50, further comprising:
a sync mark transceiver that transmits or receives sync mark information.

290. (New) The latency-independent interface of claim 289, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark

insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

291. (New) The latency-independent interface of claim 51, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

292. (New) The latency-independent interface of claim 51, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

293. (New) The latency-independent interface of claim 51, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

294. (New) The latency-independent interface of claim 51, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

295. (New) The latency-independent interface of claim 51, further comprising:

a sync mark transceiver that transmits or receives sync mark information.

296. (New) The latency-independent interface of claim 295, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

297. (New) The latency-independent interface of claim 53, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

298. (New) The latency-independent interface of claim 53, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

299. (New) The latency-independent interface of claim 53, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

300. (New) The latency-independent interface of claim 53, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

301. (New) The latency-independent interface of claim 53, further comprising:

a sync mark transceiver that transmits or receives sync mark information.

302. (New) The latency-independent interface of claim 301, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

303. (New) The method of claim 80, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

304. (New) The method of claim 80, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

305. (New) The method of claim 80, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write

padding data; and

during a read operation, information that a sync mark was detected.

306. (New) The method of claim 80, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

307. (New) The method of claim 80, further comprising the step of:

transmitting or receiving sync mark information.

308. (New) The method of claim 307, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

309. (New) The method of claim 81, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

310. (New) The method of claim 81, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

311. (New) The method of claim 81, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

312. (New) The method of claim 81, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

313. (New) The method of claim 81, further comprising the step of:

transmitting or receiving sync mark information.

314. (New) The method of claim 313, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

315. (New) The method of claim 83, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

316. (New) The method of claim 83, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

317. (New) The method of claim 83, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

318. (New) The method of claim 83, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

319. (New) The method of claim 83, further comprising the step of:

transmitting or receiving sync mark information.

320. (New) The method of claim 319, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

321. (New) The data transmission system of claim 125, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

322. (New) The data transmission system of claim 125, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

323. (New) The data transmission system of claim 125, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

324. (New) The data transmission system of claim 125, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

325. (New) The data transmission system of claim 125, wherein the first component further comprises a first sync mark transceiver that transmits or receives sync mark information, and

wherein the second component further comprises a second sync mark transceiver that transmits or receives the sync mark information.

326. (New) The data transmission system of claim 325, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

327. (New) The data transmission system of claim 126, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

328. (New) The data transmission system of claim 126, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

329. (New) The data transmission system of claim 126, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

330. (New) The data transmission system of claim 126, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

331. (New) The data transmission system of claim 126, wherein the first component further comprises a first sync mark transceiver that transmits or receives sync mark information, and

wherein the second component further comprises a second sync mark transceiver that transmits or receives the sync mark information.

332. (New) The data transmission system of claim 331, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

333. (New) The data transmission system of claim 128, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

334. (New) The data transmission system of claim 128, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

335. (New) The data transmission system of claim 128, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write

padding data; and

during a read operation, information that a sync mark was detected.

336. (New) The data transmission system of claim 128, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

337. (New) The data transmission system of claim 128, wherein the first component further comprises a first sync mark transceiver that transmits or receives sync mark information, and

wherein the second component further comprises a second sync mark transceiver that transmits or receives the sync mark information.

338. (New) The data transmission system of claim 331, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

339. (New) The method of claim 155, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

340. (New) The method of claim 155, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

341. (New) The method of claim 155, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

342. (New) The method of claim 155, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

343. (New) The method of claim 155, further comprising the steps of:
transmitting or receiving sync mark information by the first component; and
transmitting or receiving the sync mark information by the second component.

344. (New) The method of claim 343, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

345. (New) The method of claim 156, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

346. (New) The method of claim 156, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

347. (New) The method of claim 156, wherein the serial control data signal comprises:
during a write operation, information as to a start of a sync mark and a start of write padding data; and
during a read operation, information that a sync mark was detected.

348. (New) The method of claim 156, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

349. (New) The method of claim 156, further comprising the steps of:
transmitting or receiving sync mark information by the first component; and
transmitting or receiving the sync mark information by the second component.

350. (New) The method of claim 349, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

351. (New) The method of claim 158, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

352. (New) The method of claim 158, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

353. (New) The method of claim 158, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

354. (New) The method of claim 158, wherein said first hardware component comprises a disk controller and said second hardware component comprises a read channel.

355. (New) The method of claim 158, further comprising the steps of:

transmitting or receiving sync mark information by the first component; and

transmitting or receiving the sync mark information by the second component.

356. (New) The method of claim 355, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

357. (New) The latency-independent interface of claim 1, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

358. (New) The latency-independent interface of claim 1, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

359. (New) The latency-independent interface of claim 1, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

360. (New) The latency-independent interface of claim 1, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

361. (New) The latency-independent interface of claim 1, further comprising:

a sync mark transceiver that transmits or receives sync mark information.

362. (New) The latency-independent interface of claim 361, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

363. (New) The method of claim 31, wherein the serial control data signal comprises an amount of the data to be written during a write operation.

364. (New) The method of claim 31, wherein the serial control data signal comprises an amount of the data to be read during a read operation.

365. (New) The method of claim 31, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write

padding data; and

during a read operation, information that a sync mark was detected.

366. (New) The method of claim 31, wherein the first hardware component comprises a disk controller and the second hardware component comprises a read channel.

367. (New) The method of claim 31, further comprising the step of:

transmitting or receiving sync mark information.

368. (New) The method of claim 367, wherein during a write operation a first assertion of the sync mark information indicates a start of sync mark insertion and a second assertion of the sync mark information indicates a start of writing of padding data.

369. (New) The latency-independent interface of claim 46, wherein the serial control data signal comprises one of an amount of the data to be written during a write operation and an amount of the data to be read during a read operation.

370. (New) The latency-independent interface of claim 46, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

371. (New) The method of claim 76, wherein the serial control data signal comprises one of an amount of the data to be written during a write operation and an amount of the data to be read during a read operation.

372. (New) The method of claim 76, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write

padding data; and

during a read operation, information that a sync mark was detected.

373. (New) The data transmission system of claim 121, wherein the serial control data signal comprises one of an amount of the data to be written during a write operation and an amount of the data to be read during a read operation.

374. (New) The data transmission system of claim 121, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.

375. (New) The method of claim 151, wherein the serial control data signal comprises one of an amount of the data to be written during a write operation and an amount of the data to be read during a read operation.

376. (New) The method of claim 151, wherein the serial control data signal comprises:

during a write operation, information as to a start of a sync mark and a start of write padding data; and

during a read operation, information that a sync mark was detected.